AMENDMENTS TO THE SPECIFICATION

At page 1, line 3, please replace the existing paragraph with the following amended paragraph:

-- RELATED APPLICATION

This application ~~claims the benefit~~ is a divisional of U.S. Provisional Application No. 60/110,705, filed December 3, 1998 and copending U.S. Application No. 09/452,904, filed ~~on~~ December 1, 1999. --

At page 1, line 19, please replace the existing paragraph with the following amended paragraph:

--Wireless loudspeakers have existed for some time ~~[Recoton Patent Reference]~~ [U.S. Pat. No. 4,829,570 to Schotz]. The analog FM transmission systems used in these speakers have resulted in relatively low-fidelity systems with signal to noise rations on the order of 40dB to 60dB. A need exists for a high fidelity wireless loudspeaker system with performance on a par with wired solutions. --

At page 2, line 6, please replace the existing paragraph with the following amended paragraph:

--The sampling rate of a compact disk is 44,100 ± 16 bit samples/second. This results in a bit rate for stereo of 44,100 * 16 * 2 = 1,411,200 bits/second. To achieve reliable wireless transmission, redundancy must be introduced in the transmitted bit

stream. This redundancy supports a robust error detection and correction system. In addition, the wireless transmission system requires additional bits for framing and synchronization of data. In all, approximately three time the original bit rate, or 3 * 1,411,200 = 4,233,600 bits/second, is required to support wireless stereo. For a six channel surround sound home theater system, the bit rate triples to 3 * 4,233,600 = 12,700,800 bits/second. Achieving these bit rates can be extremely difficult. --

At page 3, line 16, please replace the existing paragraph with the following amended paragraph:

--~~An~~ A digital wireless loudspeaker system includes an audio transmission device for selecting and transmitting digital audio data and wireless speakers for receiving the data and broadcasting sound. Digital audio data together with a digital audio sample clock that synchronizes the data, comes to the audio transmission device from either a stereo compact disk or an AC-3 or MPEG-2 Audio Decoder that decodes and ~~uncompresses~~ decompresses the multichannel compressed audio stream coming from ~~the~~ a DVD motion picture disk. In the audio transmission device, a selector element selects the data and clock coming from either the CD Player or the Audio Decoder. The selected sample clock is used to clock the selected data into a framing and error protection encoding unit which generates frames of data and adds error protection. These transmission frames are clocked into an RF transmitter and transmitted to the speakers. For a stereo system there are two loudspeakers. For a typical surround sound home theater system there are six loudspeakers. Each loudspeaker contains an

RF receive antenna and an RF receiver, and performs acquisition and tracking on the RF signal generated by the single RF transmitter in the audio transmission device. The received bit stream and symbol clock are output from the RF receiver and input to a framing and error protection decoder and a sample clock generator. The recovered audio sample data and audio sample clock are input to a digital to speaker input conversion and channel selector. Status messages are included in the transmission frames to control speaker attributes such as speaker group, enabling or disabling a sub-woofer, and volume of the loudspeaker digitally. --

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At page 6, line 3, through page 8, line 6, please replace the BRIEF DESCRIPTION OF THE DRAWINGS section with the following amended BRIEF DESCRIPTION OF THE DRAWINGS:

--Figure 1A shows a block diagram of ~~the audio part~~ speakers of a home theater system according to the present invention.

Figure 1B shows a block diagram of a transmitter portion of a home theater system according to the present invention.

Figure 2A shows a block diagram of a second embodiment of speakers of the present invention.

Figure 2B shows a block diagram of a second embodiment of the transmitter portion of the present invention.

Figure 3 shows a detailed block diagram of the RF Receiver of Figure 1A.

Figure 4 shows a detailed block diagram of the RF Transmitter of Figure 1B.

Figure 5 shows a detailed block diagram of the Framing and Error Protection Encoding unit of Figure 1B.

Figure 6 shows a block diagram of the Framing and Error Protection Encoding unit of Figure 2B.

Figure 7 shows the diverse antenna of Figure 3 in more detail.

Figure 8 shows a block diagram of the Framing and Error Protection Decoder and Sample Clock Generator of Figure 1A.

Figure 9 shows a block diagram of the Framing and Error Protection Decoder and Clock Generator of Figure 2A.

Figure 10 shows a block diagram of one embodiment of the Speaker Input Conversion and Channel Selector of Figure 1A.

Figure 11 shows another embodiment of the Digital to Speaker Input Conversion and Channel Selector of Figure 1A.

Figure 12 shows a block diagram of the Digital to Speaker Input Conversion and Compressed Audio Decoder and Channel Selector unit of Figure 2A.

Figure 13 shows another embodiment of the Digital to Speaker Input Conversion and Compressed Audio Decoder and Channel Selector unit of Figure 2A.

Figure 14 shows one embodiment of a single channel of the Stereo Digital Audio Encoder of Figure 2B.

Figure 15A shows speakers of a third embodiment of the current invention.

Figure 15B shows a transmitter portion of a third embodiment of the current invention.

Figure 16 shows one embodiment of the RF Receiver used in the embodiment of

Figure 15A.

Figure 17 shows another embodiment of the RF Receiver used in the embodiment of Figure 15A.

Figure 18 shows one embodiment of the Channel Selection Interface of Figure 15A.

Figure 19 shows a second embodiment of the Channel Selector Interface of Figure 15A.--

At page 8, line 8, please replace the existing paragraph with the following amended paragraph:

~~--Figure 1 shows a block diagram~~ Figures 1A and 1B show block diagrams of the audio part of a home theater system in which the present invention is used. Digital Audio Data together with a digital audio Sample Clock that synchronizes the data, comes from either a stereo compact disk 135, or the AC-3 or MPEG-2 Audio Decoder 133 that decodes and ~~uncompresses~~ decompresses the multichannel compressed audio stream coming from the DVD motion picture disk 134. Audio from the DVD disk is encoded in a compressed multichannel format - generally either AC-3 six channel or MPEG-2 multichannel formats. The Selector 132 selects the Digital Audio Data and Sample Clock coming from either the CD Player 135 or the AC-3 or MPEG-2 Audio Decoder 133. The selected Sample Clock is used to clock the selected Digital Audio Data into the Framing and Error Protection Encoding unit 136.--

At page 9, line 24, please replace the existing paragraph with the following amended paragraph:

--In Figure 1B, the Transmission Frames from the Framing and Error Protection Encoding unit 136 are clocked into the RF Transmitter 131. Figure 4 shows a detailed block diagram of the RF Transmitter. In the embodiment of Figure 4, the Transmission Frames output from 136 form a bit stream that is input to the Modulator and Direct Sequence Spread Spectrum (DSSS) Spreader 405. The Modulator and DSSS Spreader 405 takes the input bit stream M bits at a time and generates M-ary symbols. The symbols are generated at the Symbol Rate which is equal to the input bit rate divided my M. M is the number of bits per symbol and is typically in the range 2 to16. The symbols are modulated by a spreading sequence. The spreading sequence modulation, called the Chip Rate, is S times the symbol rate. S is typically in the range 10 to 16.--

At page 12, line 6, please replace the existing paragraph with the following amended paragraph:

-- In another embodiment both the Chip Clock and Symbol Clock and the Sample Clock are generated by frequency multiplication and clock division from the same Clock Oscillator running from the same crystal or frequency source. In general this oscillator ~~run~~ runs at a high frequency so that only clock dividers are required to generate both the Symbol Clock, Chip Clock, and audio Sample Clock. --

At page 12, line 12, please replace the existing paragraph with the following amended paragraph:

-- The interleave function performed by the Reed Solomon Encoder and Interleaver 502 with Frame Marker Insertion ~~407~~ 501 protects against burst errors by scrambling adjacent bits across multiple Reed Solomon encoding blocks. This error protection system is ~~a~~ called a concatenated encoder with interleaving and is well known to those skilled in the art of error protection system design [*Error Control Coding: Fundamental and Applications, Lin and Costelle, Prentice Hall, 1983*]. --

At page 14, line 18, please replace the existing paragraph with the following amended paragraph:

--Figure 1A shows Loudspeaker One 100, Loudspeaker Two 110 and Loudspeaker N 120. For a stereo system there are two loudspeakers. For a typical surround sound home theater system there are six loudspeakers. It is clear to one skilled in the art that the present invention can accommodate any reasonable number of loudspeakers with N typically equal to 2 through 8.--

At page 16, line 7, please replace the existing paragraph with the following amended paragraph:

-- In the RF receiver embodiment of Figure 3, the RF frequency signal from the antenna 300 is input to the RF Low Noise Amplifier 301 whose output is sent to the RF Downconverter 302. The RF Downconverter 302 modulates the RF signal, using a sinusoid generated by the RF VCO 310, down to IF frequency. Some details such as band pass and low pass filters are left out of the block diagram of Figure 3. Those skilled in the art of RF System design will recognize this and understand that only the principle blocks of the RF receiver design are shown in Figure 3. The IF signal is further down modulated by the IF Demodulator 303 using a signal generated by the IF VCO 309. The output of the IF Demodulator is a complex signal consisting of I and Q -- real, imaginary -- running at the Chip Rate. The I and Q components are input to an Analog to Digital Converter (ADC) 304 with sampling rate typically 1-2 times the Chip Rate. The ADC precision is typically 3 to 4 bits for I, and 3 to 4 bits for Q. In order to successfully decode the received I and Q signals, they must be despread. This is accomplished by again multiplying I and Q with the same spreading sequence used in the Modulator and DSSS Spreader 405 of the RF transmitter. This spreading sequence is known in advance. The spreading sequence must be correctly aligned in time with the received I and Q signals. This process is called symbol synchronization and is generally accomplished in two stages: a course synchronization stage called acquisition, and a fine tuning synchronization stage called tracking. Synchronization is implemented by the Correlator, DSSS Despreader and Demodulator with Acquisition and Tracking for Symbol Synchronization 305. Separate despreaders and correlators are used for the I and Q components. The correlators multiply the input I and Q signals with the spreading sequence. The multiply and sum operation of the correlators is done

at a series of different delays with respect to the maximum correlation value. At this delay the input I and Q signals are roughly synchronized with the Symbol Rate of the transmitter. The corresponds to the output of the acquisition stage of symbol synchronization. The symbol synchronization is further fine tuned by a tracking stage. Several techniques for tracking are known in the art. These include Delay-Locked Loop (DLL) and Tau-Dither Loop techniques. [*Digital Communications, Fundamentals and Applications, Benard Sklar, Prentice Hall, 1988*]. Acquisition and tracking allow the start of the symbol period to be known with excellent sub-chip period resolution. At the start of each symbol period, as determined by the acquisition and tracking stages, the Correlator, DSSS Despreader and Demodulator with Acquisition and Tracking for Symbol Synchronization 305 outputs a pulse. This stream of pulses, once per symbol, is the Symbol Clock. Similar acquisition and tracking techniques are used to perform Symbol Synchronization in FHSS systems and, in fact, in every other Digital RF Transmission system. Symbol synchronization techniques are well known to those skilled in the art of RF Receiver design and it is obvious to such a practitioner that the particular type of Symbol Synchronization employed will not change the character of the present invention. --

At page 18, line 18, please replace the existing paragraph with the following amended paragraph:

--In Figure 1A we see that the received bit stream and Symbol Clock are output from the RF Receiver and input to the Framing and Error Protection Decoder and

Sample Clock Generator 106, 116, 126. A block diagram of the Framing and Error Protection Decoder and Sample Clock Generator is shown in Figure 8. The received bit stream is input to the Viterbi Decoder 800 which performs error detection and correction corresponding to the Convolutional Encoder 500 of Figure 5. The Viterbi decoded bit stream is input to the Frame Synchronizer 801.--

At page 21, line 6, please replace the existing paragraph with the following amended paragraph:

--As shown in Figure 1A, the recovered Audio Sample Data and Audio Sample Clock are input to the Digital to Speaker Input Conversion and Channel Selector 103, 113, 123. A block diagram of one embodiment of the Speaker Input Conversion and Channel Selector is shown in Figure 10. The Digital Audio Sample Data input to Figure 10 consists of all channels of audio.--

At page 21, line 12, please replace the existing paragraph with the amended paragraph below:

-- The output of the Channel Selection Interface 1000 determines which audio channel the individual loudspeaker is assigned to in a surround sound or stereo system, which mix mode to use (described later), and digital crossover filter EQ information (also described later). Figure 18 shows one embodiment of the Channel Selection Interface. A Channel Selection Switch 1801 located on the speaker cabinet allows the user to

specify what role an individual speaker is assigned to in a surround sound system: left front, center front, right front, left read, right rear. In the case of subwoofer the speaker itself is sufficiently distinctive that ~~knew~~ no switch is necessary. The output of the Channel Selection Switch is input to the Channel Selection Register and Status Decode Logic 1802. The output of the Channel Selection Register and Status Decode Logic 1802 is the output of the Channel Selection Interface 1000 and is sent to the remaining functional units of the Digital to Speaker Input Conversion and Channel Selector. A special NO_CHANNEL output code from the Channel Selection Interface specifies that the speaker is disabled and should respond to no channel selection. Also comprised in the Channel Selection Interface is a Group Selection Switch 1800. Many homes and offices have multiple groups of loudspeakers - e.g. a group of loudspeakers in the living room and another group in the kitchen. The Group Selection Switch allows a loudspeaker to be assigned to one of many groups of loudspeakers. --

At page 22, line 10, please replace the existing paragraph with the following amended paragraph:

--Status information from the Framing and Error Protection Decoder and Sample Clock Generator 106, 116, 126 of Figure 1A is also received by the Channel Selection Interface 1000 and input to the Channel Selection Register and Status Decode Logic 1802. Among other messages, the status information contains commands to enable or disable a particular group of speakers. When the group to which the current loudspeaker is assigned is disabled, the Channel Selection Register and Status

Decoder Logic 1802 is set to output the special NO_CHANNEL output code.--

At page 24, line 17, please replace the existing paragraph with the following amended paragraph:

--The multichannel audio sample is input to the Channel Selector and Mixer and Volume Control 1003 which selects one channel from the multichannel Digital Audio Sample Data input, or mixes several channels of a surround sound signal to one channel, and outputs this to the Digital Crossover Filter 1004. In the embodiment shown in Figure 1A a two way loudspeaker system is used, and so, the Digital Crossover 1004 divides the digital audio signal into a low and high frequency output. In another embodiment a three or four way system is used and the digital crossover divides the digital audio signal into three or four bands. There are a number of advantages to using digital filtering for implementing the crossover function. With digital filtering accurate linear phase filters can be designed. In addition the digital filters can be made to compensate for the non ideal phase and magnitude frequency characteristics of the speakers themselves. In addition the digital filter coefficients for the Digital Crossover 1004 can be downloaded to the loudspeaker using the status information which is decoded and output by the Channel Selection Interface 1000. These coefficients can be specially adjusted to compensate for acoustic differences in the room that the loudspeakers are placed in or can be adjusted according to whether or not a sub-woofer is present in the system. Different size and shapes of rooms and the locations of loudspeakers placed in them result in different, and often undesirable,

changes in frequency response for a loudspeaker system. These can be almost eliminated using by using downloadable filter coefficients for the Digital Crossover 1004. The low and high frequency digital signals output from the Digital Crossover 1004 are input to two digital to analog converters (DACs) 1005, 1006. The analog outputs of the DACs 1005, 1006 are input to a Low Frequency Power Amplifier 1008 that drives the Woofer (101, 111, 121 in Figure 1A), and a High Frequency Power Amplifier 1007 that drives the Tweeter (102, 112, 122 in Figure 1A).--

At page 27, line 12, please replace the existing paragraph with the following amended paragraph:

--Both the embodiments of Figure 10 and Figure 11 require a Sample Clock to synchronize the incoming audio sample data and subsequent units that operate on the data. The Sample Clock is generated by the Framing and Error Decoder and Sample Clock Generator as shown in Figure 1A.--

At page 27, line 17, please replace the existing paragraph with the amended paragraph below:

-- In the embodiment of Figure 1A, the function of channel selection is performed in the Digital to Speaker Input Conversion and Channel Selector unit 103, 113, 123. This corresponds to a Time Domain Multiple Access (TDMA) method of multiplexing the multiple audio channels onto a single RF frequency carrier. ~~Figure 15 shows~~ Figures

15A and 15B show another embodiment of the current invention. In this embodiment the function of channel selection is performed in the RF Receiver 1504, 1514, 1524 rather than in the Digital to Speaker Input Conversion Unit 1503, 1513, 1523. Figure 16 shows one embodiment of the RF Receiver, which is similar to the RF Receiver of Figure 3 and is used in the embodiment of Figure 15A. Here the output of the Channel Selection Register 1613, whose value is set by the Channel Selection Switch 1611, sets the RF carrier frequency and the RF Transmitter 1531 transmits each audio channel on a separate carrier frequency. This corresponds to a Frequency Domain Multiple Access (FDMA) method of multiplexing the multiple audio channels. As shown in the embodiment of Figure 16, the Channel Selection register sets the carrier frequency of both the RF Downconverter 1602 and IF Quadrature Demodulators 1603. In another embodiment, only the carrier frequency of the IF Quadrature Demodulator 1603 is set by the Channel Selection Register 1613. Figure 17 shows another embodiment of the RF Receiver, which is similar to the RF Receiver of Figure 3 and is used in embodiment of Figure 15A. In this embodiment, the Channel Selection Register 1713 sets the spreading code for the RF Receiver. This corresponds to a Code Division Multiple Access (CDMA) method of multiplexing the multiple audio channels. Corresponding to the RF Receiver embodiment of Figure 17, the RF Transmitter 1531 transmits the multiple audio channels using different spreading codes. --

At page 28, line 21, please replace the existing paragraph with the following amended paragraph:

--In the embodiment of the present invention shown in Figure 15A, the Channel Selection Switch 1611, 1711 is moved into the RF Receiver so that it can set the RF carrier frequency and subcarrier frequencies or the spreading code. This results in a new embodiment of the Digital to Speaker Input Conversion unit 1503, 1513, 1523. This embodiment is identical to the embodiments of Digital to Speaker Input Conversion and Channel Selector described above for Figure 1A, 103, 113, 123, except that a new embodiment of Channel Selector Interface is used. This Channel Selector Interface embodiment is shown in Figure 19. It is the same as that for Figure 18 except with no Channel Selection Switch. In this embodiment of the Channel Selector Interface no actual channel selection is performed, just status decoding and group selection switching, however the name is retained for continuity.--

At page 29, line 10, please replace the existing paragraph with the following amended paragraph:

-- The block ~~diagram of Figure 2 shows~~ diagrams of Figures 2A and 2B show another embodiment of the present invention, which is similar to the embodiment of Figures 1A and 1B. In this embodiment, the digital audio sample stream is digitally compressed before it is transmitted through the air. At the loudspeaker, the compressed digital audio sample stream is uncompressed and a single channel of uncompressed audio is output to the speaker. By transmitting digitally compressed audio the bit rate required for RF transmission is reduced, greatly simplifying the RF design. --

At page 33, line 3, please replace the existing paragraph with the following amended paragraph:

-- Just as in Figure 1A, each loudspeaker ~~in~~ 200,210,220 in Figure 2A has an Antenna 205,215,225 and RF Receiver 204,214,~~223~~ 224 which are identical with those of Figure 1A. The output of the RF Receivers is input to the Framing and Error Protection Decoder and Clock Generator 206, 216, 226. A block diagram of the Framing and Error Protection Decoder and Clock Generator is shown in Figure 9. The functions of Figure 9 are mostly identical with the functions of Figure 8 described for the non-compressed audio case. The difference is that the output of the Deinterleaver 904 is a bit stream consisting of Compressed Digital Audio Frame Data whose boundaries are marked by the Compressed Digital Audio Frame Clock which is also output from the Deinterleaver 904. The Compressed Audio Bit Clock and Audio Sample Clock Generater 905 functions much like its counterpart 805 in Figure 8 except that in addition to regenerating the Audio Sample Clock it also regenerates the Compressed Digital Audio Bit Clock to synchronize the bits coming from the Deinterleaver. Figure 13 shows another embodiment of the Digital to Speaker Input Conversion and Compressed Audio Decoder and Channel Selector unit. --

At page 33, line 22, please replace the existing paragraph with the following amended paragraph:

--In the embodiment of Figure 2A, the output of the Framing and Error Protection Decoder and Clock Generator 206, 216, 226, consisting of Compressed Audio Frame and Bit Clocks Audio Sample Clock and Compressed Audio bit stream, is input to the Digital to Speaker Input Conversion and Compressed Audio Decoder and Channel Selector unit 203, 213, 223.--

At page 35, line 12, please replace the existing paragraph with the following amended paragraph:

-- Figure 13 shows another embodiment of the Digital to Speaker Input Conversion and Compressed Audio Decoder and Channel Selector unit. The embodiment of Figure 13 has the same Bit Field Extraction and Channel Selection Unit 1203 and Dequantize Frequency Band Bit Fields and Rescale to Linear Frequency Scale and Mixing and Volume Control Unit 1204 as in Figure 12. In this embodiment, the digital crossover function is implemented as a Frequency Domain Digital Crossover 1305 before the data is inverse transformed to the time domain. This is a particular economical implementation of the crossover function. Crossover coefficient, this time in the frequency domain, can be set by the Channel Selection Interface 1300. The frequency domain digital crossover results in separate frequency domain data blocks for the high frequency and low frequency bands. These blocks are separately inverse transformed 1306, 1308 and overlap added 1307, 1309 ~~two~~ to generate the high and low frequency digital time domain signals which are the input to the high and low frequency DACs 1310, 1312 and then the high and low frequency power amplifiers 1311, 1313. The

DACs and power amplifiers of Figure 13 can be replaced by Class D digital input amplifiers as in Figure 12. --

At page 36, line 3, please replace the existing paragraph with the following amended paragraph:

-- The embodiments of Figure 12 and Figure 13 have the same auto power on/off embodiments 1214 and 1314 as those of Figure 10 described earlier. --

At page 36, line 6, please replace the existing paragraph with the following amended paragraph:

-- The embodiments of Figure 12 and Figure 13 require a Compressed Audio Frame Clock, a Compressed Audio Bit Clock, and an uncompressed Sample Clock to synchronize the incoming compressed audio data sample data and later the uncompressed sampled data. These clocks are generated by the Framing and Error Protection Decoder and Clock Generator as shown in Figures 1A, 1B, 2A and 2B. --

At page 36, line 19, please replace the existing paragraph with the following amended paragraph:

--In both the uncompressed and compressed embodiments of Figure 1A and Figure 2A, the RF Receivers in each loudspeaker are designed to function in one of the unlicensed Instrumentation, Scientific, and Medical (ISM) frequency bands defined by the FCC in the U.S. These bands are centered around 900 MHz, 2.4 GHz, and 5.7 GHz. Internationally 900 MHz is not available for this type of product. Whatever transmission frequency band is used the important thing is that the bandwidth be

sufficient to support the transmitted bit streams as described above. It is obvious to one skilled in the art that almost any transmission band can, in theory, be used for this purpose as long as bandwidth is sufficient. In particular, embodiments for different countries will no doubt use different transmission bands.--